[RC Tech & LEF files for skywater 130nm](https://github.com/Subhasis-Sahu/SFAL-VSD/commit/d21fdb1d1aaef2f45ccd263b8339753a754dcfc2)

module vsdbabysoc (

output wire OUT,

//

input wire reset,

//

/\*input wire VCO\_IN,

input wire ENb\_CP,\*/

input wire ENb\_VCO,

input wire REF,

//

// input wire VREFL,

input wire VREFH

);

wire CLK;

wire [9:0] RV\_TO\_DAC;

rvmyth core (

.OUT(RV\_TO\_DAC),

.CLK(CLK),

.reset(reset)

);

/\*avsdpll pll (

.CLK(CLK),

.VCO\_IN(VCO\_IN),

.ENb\_CP(ENb\_CP),

.ENb\_VCO(ENb\_VCO),

.REF(REF)

);\*/

pll pll\_1 (

.f\_vco(CLK),

.vctrl(ENb\_VCO),

.f\_clk\_in(REF)

);

avsddac dac (

.OUT(OUT),

.D(RV\_TO\_DAC),

// .VREFL(VREFL),

.VREFH(VREFH)

);